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This book addresses key aspects of analog integrated circuits and systems design related to system level electrostatic discharge (ESD) protection. It is an invaluable reference for anyone developing systems-on-chip (SoC) and systems-on-package (SoP), integrated with system-level ESD protection. The book focuses on both the design of semiconductor integrated circuit (IC) components with embedded, on-chip system level protection and IC-system co-design. The readers will be enabled to bring the system level ESD protection solutions to the level of integrated circuits, thereby reducing or completely eliminating the need for additional, discrete components on the printed circuit board (PCB) and meeting system-level ESD requirements. The authors take a systematic approach, based on IC-system ESD protection co-design. A detailed description of the available IC-level ESD testing methods is provided, together with a discussion of the correlation between IC-level and system-level ESD testing methods. The IC-level ESD protection design is demonstrated with representative case studies which are analyzed with various numerical simulations and ESD testing. The overall methodology for IC-system ESD co-design is presented as a step-by-step procedure that involves both ESD testing and numerical simulations.

Electrostatic discharge (ESD) continues to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a whole-chip ESD design synthesis approach. It provides a clear insight into the integration of ESD protection networks from a generalist perspective, followed by examples in specific technologies, circuits, and chips. Uniquely both the semiconductor chip integration issues and floorplanning of ESD networks

are covered from a ‘top-down' design approach. Look inside for extensive coverage on: integration of cores, power bussing, and signal pins in DRAM, SRAM, CMOS image processing chips, microprocessors, analog products, RF components and how the integration influences ESD design and integration architecturing of mixed voltage, mixed signal, to RF design for ESD analysis floorplanning for peripheral and core I/O designs, and the implications on ESD and latchup guard ring integration for both a ‘bottom-up' and ‘top-down' methodology addressing I/O guard rings, ESD guard rings, I/O to I/O, and I/O to core classification of ESD power clamps and ESD signal pin circuitry, and how to make the correct choice for a given semiconductor chip examples of ESD design for the state-of-the-art technologies discussed, including CMOS, BiCMOS, silicon on insulator (SOI), bipolar technology, high voltage CMOS (HVCMOS), RF CMOS, and smart power practical methods for the understanding of ESD circuit power distribution, ground rule development, internal bus distribution, current path analysis, quality metrics ESD: Design and Synthesis is a continuation of the author's series of books on ESD protection. It is an essential reference for: ESD, circuit, and semiconductor engineers; design synthesis team leaders; layout design, characterisation, floorplanning, test and reliability engineers; technicians; and groundrule and test site developers in the manufacturing and design of semiconductor chips. It is also useful for graduate and undergraduate students in electrical engineering, semiconductor sciences, and manufacturing sciences, and on courses involving the design of ESD devices, chips and systems. This book offers a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

The book all semiconductor device engineers must read to gain a practical feel for latchup-induced failure to produce lower-cost and higher-density chips. Transient-Induced Latchup in CMOS Integrated Circuits equips the practicing engineer with all the tools needed to address this regularly occurring problem while becoming more proficient at IC layout. Ker and Hsu introduce the phenomenon and basic physical mechanism of latchup, explaining the critical issues that have resurfaced for CMOS technologies. Once readers can gain an understanding of the standard practices for TLU, Ker and Hsu discuss the physical mechanism of TLU under a system-level ESD test, while introducing an efficient component-level TLU measurement setup. The authors then present experimental methodologies to extract safe and area-efficient compact layout rules for latchup prevention, including layout rules for I/O cells, internal circuits, and between I/O and internal circuits. The book concludes with an appendix giving a practical example of extracting layout rules and guidelines for latchup prevention in a 0.18-micrometer 1.8V/3.3V silicided CMOS process. Presents real cases and solutions that occur in commercial CMOS IC chips Equips engineers with the skills to conserve chip layout area and decrease time-to-market Written by experts with real-world experience in circuit design and failure analysis Distilled from numerous courses taught by the authors in IC design houses worldwide The only book to introduce TLU under system-level ESD and EFT tests This book is essential for practicing engineers involved in IC design, IC design management, system and application design, reliability, and failure analysis. Undergraduate and postgraduate students, specializing in CMOS circuit design and layout, will find this book to be a valuable introduction to real-world industry

problems and a key reference during the course of their careers.
Radio Design in Nanometer Technologies is the first volume that looks at the integrated radio design problem as a "piece of a big puzzle", namely the entire chipset or single chip that builds an entire wireless system. This is the only way to successfully design radios to meet the stringent demands of today’s increasingly complex wireless systems.

Esd in Silicon Integrated Circuits Ajith Amerasekera Charvaka Duvvury Texas Instruments Inc, Dallas, USA Electrostatic Discharge (ESD) effects in silicon integrated circuits have become a major concern as today's high circuit density technologies shrink to sub-micro dimensions. This book provides an understanding of the basic features related to ESD and deals with topics ranging from the physics of devices operating under ESD conditions to approaches for solving and improving ESD performance in advanced ICs. Features include: * Description of the methods used to reproduce ESD-type events in a controlled test environment * Analysis of the behavior of different semiconductor devices under ESD conditions, including the physics and modeling of devices * Detailed study of design and layout requirements for ESD protection circuits * Case studies showing examples of approaches to solving ESD design problems, including failure analysis Covering the state-of-the-art in circuit design for ESD prevention, this practical book is written from an industrial perspective and will appeal to engineers and scientists working in the fields of IC and transistor design. Researchers and advanced students in the fields of device/circuit modeling and semiconductor reliability, seeking to understand the fundamentals of ESD phenomena, will also find this book an invaluable reference source.
A practical and comprehensive reference that explores Electrostatic Discharge (ESD) in semiconductor components and electronic systems The ESD Handbook offers a comprehensive reference that explores topics relevant to ESD design in semiconductor components and explores ESD in various systems. Electrostatic discharge is a common problem in the semiconductor environment and this reference fills a gap in the literature by discussing ESD protection. Written by a noted expert on the topic, the text offers a topic-by-topic reference that includes illustrative figures, discussions, and drawings. The handbook covers a wide-range of topics including ESD in manufacturing (garments, wrist straps, and shoes); ESD Testing; ESD device physics; ESD semiconductor process effects; ESD failure mechanisms; ESD circuits in different technologies (CMOS, Bipolar, etc.); ESD circuit types (Pin, Power, Pin-to-Pin, etc.); and much more. In addition, the text includes a glossary, index, tables, illustrations, and a variety of case studies. Contains a well-organized reference that provides a quick review on a range of ESD topics Fills the gap in the current literature by providing information from purely scientific and physical aspects to practical applications Offers information in clear and accessible terms Written by the accomplished author of the popular ESD book series Written for technicians, operators, engineers, circuit designers, and failure analysis engineers, The ESD Handbook contains an accessible reference to ESD design and ESD systems.
This comprehensive and insightful book discusses ESD protection circuit design problems from an IC designer's perspective. On-Chip ESD Protection for Integrated Circuits: An IC Design Perspective provides both fundamental and advanced materials needed

by a circuit designer for designing ESD protection circuits, including: Testing models and standards adopted by U.S. Department of Defense, EIA/JEDEC, ESD Association, Automotive Electronics Council, International Electrotechnical Commission, etc. ESD failure analysis, protection devices, and protection of sub-circuits Whole-chip ESD protection and ESD-to-circuit interactions Advanced low-parasitic compact ESD protection structures for RF and mixed-signal IC's Mixed-mode ESD simulation-design methodologies for design prediction ESD-to-circuit interactions, and more! Many real world ESD protection circuit design examples are provided. The book can be used as a reference book for working IC designers and as a textbook for students in the IC design field.

"This book provide a comprehensive coverage of the latest and most relevant knowledge, developments, solutions, and practical applications, related to e-Health, this new field of knowledge able to transform the way we live and deliver services, both from the technological and social perspectives"--Provided by publisher.

An authoritative single-volume reference on the design and analysis of ESD protection for ICs Electrostatic discharge (ESD) is a major reliability challenge to semiconductors, integrated circuits (ICs), and microelectronic systems. On-chip ESD protection is a vital to any electronic products, such as smartphones, laptops, tablets, and other electronic devices. Practical ESD Protection Design provides comprehensive and systematic guidance on all major aspects of designs of on-chip ESD protection for integrated circuits (ICs). Written for students and practicing engineers alike, this one-stop resource covers essential theories, hands-on design skills, computer-aided design (CAD) methods, characterization and analysis techniques, and more on ESD protection designs. Detailed chapters examine an array of topics ranging from fundamental to advanced, including ESD phenomena, ESD failure analysis, ESD testing models, ESD protection devices and circuits, ESD design layout and technology effects, ESD design flows and co-design methods, ESD modelling and CAD techniques, and future ESD protection concepts. Based on the author’s decades of design, research and teaching experiences, Practical ESD Protection Design: • Features numerous real-world ESD protection design examples • Emphasizes on ESD protection design techniques and procedures • Describes ESD-IC co-design methodology for high--performance mixed-signal ICs and broadband radio-frequency (RF) ICs • Discusses CAD-based ESD protection design optimization and prediction using both Technology and Electrical Computer-Aided Design (TCAD/ECAD) simulation • Addresses new ESD CAD algorithms and tools for full-chip ESD physical design verification • Explores the disruptive future outlook of ESD protection Practical ESD Protection Design is a valuable reference for industrial engineers and academic researchers in the field, and an excellent textbook for electronic engineering courses in semiconductor microelectronics and integrated circuit designs.

As we enter the nanoelectronics era, electrostatic discharge (ESD) phenomena is an important issue for everything from micro--electronics to nanostructures. This book provides insight into the operation and design of micro-gaps and nanogenerators with chapters on low capacitance ESD design in advanced technologies, electrical breakdown in micro-gaps, nanogenerators from ESD, and theoretical prediction and optimization of triboelectric

nanogenerators. The information contained herein will prove useful for for engineers and scientists that have an interest in ESD physics and design.

The book gathers a collection of high-quality peer-reviewed research papers presented at the International Conference on Information System Design and Intelligent Applications (INDIA 2018), which was held at the Universite des Mascareignes, Mauritius from July 19 to 21, 2018. It covers a wide range of topics in computer science and information technology, from image processing, database applications and data mining, to grid and cloud computing, bioinformatics and many more. The intelligent tools discussed, e.g. swarm intelligence, artificial intelligence, evolutionary algorithms, and bio-inspired algorithms, are currently being applied to solve challenging problems in various domains.

This book enables readers to design effective ESD protection solutions for all mainstream RF fabrication processes (GaAs pHEMT, SiGe HBT, CMOS). The new techniques introduced by the authors have much higher protection levels and much lower parasitic effects than those of existing ESD protection devices. The authors describe in detail the ESD phenomenon, as well as ESD protection fundamentals, standards, test equipment, and basic design strategies. Readers will benefit from realistic case studies of ESD protection for RFICs and will learn to increase significantly modern RFICs' ESD safety level, while maximizing RF performance.

* Examines the various methods available for circuit protection, including coverage of the newly developed ESD circuit protection schemes for VLSI circuits. * Provides guidance on the implementation of circuit protection measures. * Includes new sections on ESD design rules, layout approaches, package effects, and circuit concepts. * Reviews the new Charged Device Model (CDM) test method and evaluates design requirements necessary for circuit protection.

This Book and Simulation Software Bundle Project Dear Reader, this book project brings to you a unique study tool for ESD protection solutions used in analog-integrated circuit (IC) design. Quick--start learning is combined with in-depth understanding for the whole spectrum of cro- disciplinary knowledge required to excel in the ESD ?eld. The chapters cover technical material from elementary semiconductor structure and device levels up to complex analog circuit design examples and case studies. The book project provides two different options for learning the material. The printed material can be studied as any regular technical textbook. At the same time, another option adds parallel exercise using the trial version of a complementary commercial simulation tool with prepared simulation examples. Combination of the textbook material with numerical simulation experience presents a unique opportunity to gain a level of expertise that is hard to achieve otherwise. The book is bundled with simpli?ed trial version of commercial mixed- TM mode simulation software from Angstrom Design Automation. The DECIMM (Device Circuit Mixed--Mode) simulator tool and complementary to the book s- ulation examples can be downloaded from www.analogesd.com. The simulation examples prepared by the authors support the speci?c examples discussed across the book chapters. A key idea behind this project is to provide an opportunity to not only study the book material but also gain a much deeper understanding of the subject by direct experience through practical simulation exam-

ples.
An effective and cost efficient protection of electronic system against ESD stress pulses specified by IEC 61000-4-2 is paramount for any system design. This pioneering book presents the collective knowledge of system designers and system testing experts and state-of-the-art techniques for achieving efficient system-level ESD protection, with minimum impact on the system performance. All categories of system failures ranging from 'hard' to 'soft' types are considered to review simulation and tool applications that can be used. The principal focus of System Level ESD Co-Design is defining and establishing the importance of co-design efforts from both IC supplier and system builder perspectives. ESD designers often face challenges in meeting customers' system-level ESD requirements and, therefore, a clear understanding of the techniques presented here will facilitate effective simulation approaches leading to better solutions without compromising system performance. With contributions from Robert Ashton, Jeffrey Dunnihoo, Micheal Hopkins, Pratik Maheshwari, David Pomerenke, Wolfgang Reinprecht, and Matti Usumaki, readers benefit from hands-on experience and in-depth knowledge in topics ranging from ESD design and the physics of system ESD phenomena to tools and techniques to address soft failures and strategies to design ESD-robust systems that include mobile and automotive applications. The first dedicated resource to system-level ESD co-design, this is an essential reference for industry ESD designers, system builders, IC suppliers and customers and also Original Equipment Manufacturers (OEMs). Key features: Clarifies the concept of system level ESD protection. Introduces a co-design approach for ESD robust systems. Details soft and hard ESD fail mechanisms. Detailed protection strategies for both mobile and automotive applications. Explains simulation tools and methodology for system level ESD co-design and overviews available test methods and standards. Highlights economic benefits of system ESD co-design.
With the growth of high-speed telecommunications and wireless technology, it is becoming increasingly important for engineers to understand radio frequency (RF) applications and their sensitivity to electrostatic discharge (ESD) phenomena. This enables the development of ESD design methods for RF technology, leading to increased protection against electrical overstress (EOS) and ESD. ESD: RF Technology and Circuits: Presents methods for co-synthesizisng ESD networks for RF applications to achieve improved performance and ESD protection of semiconductor chips; discusses RF ESD design methods of capacitance load transformation, matching network co-synthesis, capacitance shunts, inductive shunts, impedance isolation, load cancellation methods, distributed loads, emitter degeneration, buffering and ballasting; examines ESD protection and design of active and passive elements in RF complementary metal-oxide-semiconductor (CMOS), RF laterally-diffused metal oxide semiconductor (LDMOS), RF BiCMOS Silicon Germanium (SiGe), RF BiCMOS Silicon Germanium Carbon (SiGeC), and Gallim Arsenide technology; gives information on RF ESD testing methodologies, RF degradation effects, and failure mechanisms for devices, circuits and systems; highlights RF ESD mixed-signal design integration of digital, analog and RF circuitry; sets out examples of RF ESD design computer aided design methodologies; covers state-of-the-art RF ESD input circuits, as well as voltage-triggered to RC-triggered ESD power clamps net-

works in RF technologies, as well as off-chip protection concepts. Following the authors series of books on ESD, this book will be a thorough overview of ESD in RF technology for RF semiconductor chip and ESD engineers. Device and circuit engineers working in the RF domain, and quality, reliability and failure analysis engineers will also find it a valuable reference in the rapidly growing are of RF ESD design. In addition, it will appeal to graduate students in RF microwave technology and RF circuit design.

A comprehensive and in-depth review of analog circuitlayout, schematic architecture, device, power network and ESDdesign This book will provide a balanced overview of analog circuitdesign layout, analog circuit schematic development,architecture of chips, and ESD design. It will start atan introductory level and will bring the reader right up to thestate-of-the-art. Two critical design aspects for analog and powerintegrated circuits are combined. The first design aspect coversanalog circuit design techniques to achieve the desired circuitperformance. The second and main aspect presents the additionalchallenges associated with the design of adequate and effective ESDprotection elements and schemes. A comprehensive list of practicalapplication examples is used to demonstrate the successfulcombination of both techniques and any potential designtrade-offs. Chapter One looks at analog design discipline, including layoutand analog matching and analog layout design practices. Chapter Twodiscusses analog design with circuits, examining: singletransistor amplifiers; multi-transistor amplifiers; active loadsand more. The third chapter covers analog design layout (alsoMOSFET layout), before Chapters Four and Five discuss analog designsynthesis. The next chapters introduce the reader to analog-digitalmixed signal design synthesis, analog signal pin ESD networks, andanalog ESD power clamps. Chapter Nine, the last chapter, covers ESDdesign in analog applications. Clearly describes analog design fundamentals (circuitfundamentals) as well as outlining the various ESDimplications Covers a large breadth of subjects and technologies, such asCMOS, LDMOS, BCD, SOI, and thick body SOI Establishes an “ESD analog design” discipline thatdistinguishes itself from the alternative ESD digital designfocus Focuses on circuit and circuit design applications Assessible, with the artwork and tutorial style of the ESD bookseries PowerPoint slides are available for university facultymembers Even in the world of digital circuits, analog and power circuitsare two very important but under-addressed topics, especially fromthe ESD aspect. Dr. Voldman’s new book will serve as anessential and practical guide to the greater IC community. Withhigh practical and academic values this book is a“bible” for professionals, graduate students, deviceand circuit designers for investigating the physics of ESD and forproduct designs and testing.

Neil Sclater offers practical advice on selecting test and control equipment, handling and storing semiconductors and other components, building static-free workstations, creating a protective environment for electronics, and much more. A complete listing of manufacturers and suppliers in included. Prior to founding his own electronics marketing research firm, Neil Sclater worked as an engineer for several leading corporations and as editor for Electronic Design and Product Engineering. He is the author of TPR's Gallium Arsenide IC Technology (No 3089).

ESD Protection Device and Circuit Design for Advanced CMOS

Technologies is intended for practicing engineers working in the areas of circuit design, VLSI reliability and testing domains. As the problems associated with ESD failures and yield losses become significant in the modern semiconductor industry, the demand for graduates with a basic knowledge of ESD is also increasing. Today, there is a significant demand to educate the circuits design and reliability teams on ESD issues. This book makes an attempt to address the ESD design and implementation in a systematic manner. A design procedure involving device simulators as well as circuit simulator is employed to optimize device and circuit parameters for optimal ESD as well as circuit performance. This methodology, described in ESD Protection Device and Circuit Design for Advanced CMOS Technologies has resulted in several successful ESD circuit design with excellent silicon results and demonstrates its strengths.

Electrostatic discharge (ESD) failure mechanisms continue to impact semiconductor components and systems as technologies scale from micro- to nano-electronics. This book studies electrical overstress, ESD, and latchup from a failure analysis and case-study approach. It provides a clear insight into the physics of failure from a generalist perspective, followed by investigation of failure mechanisms in specific technologies, circuits, and systems. The book is unique in covering both the failure mechanism and the practical solutions to fix the problem from either a technology or circuit methodology. Look inside for extensive coverage on: failure analysis tools, EOS and ESD failure sources and failure models of semiconductor technology, and how to use failure analysis to design more robust semiconductor components and systems; electro-thermal models and technologies; the state-of-the-art technologies discussed include CMOS, BiCMOS, silicon on insulator (SOI), bipolar technology, high voltage CMOS (HVCMOS), RF CMOS, smart power, gallium arsenide (GaAs), gallium nitride (GaN), magneto-resistive (MR) , giant magneto-resistors (GMR), tunneling magneto-resistor (TMR), devices; micro electro-mechanical (MEM) systems, and photo-masks and reticles; practical methods to use failure analysis for the understanding of ESD circuit operation, temperature analysis, power distribution, ground rule development, internal bus distribution, current path analysis, quality metrics, (connecting the theoretical to the practical analysis); the failure of each key element of a technology from passives, active elements to the circuit, sub-system to package, highlighted by case studies of the elements, circuits and system-on-chip (SOC) in today’s products. ESD: Failure Mechanisms and Models is a continuation of the author’s series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the Nano-electronic era.

Electrical Overstress (EOS) continues to impact semiconductor manufacturing, semiconductor components and systems as technologies scale from micro- to nano-electronics. This bookteaches the fundamentals of electrical overstress and how to minimize and mitigate EOS failures. The text provides a clear picture of EOS phenomena, EOS origins, EOS sources, EOS physics, EOS failure mechanisms, and EOS on-chip and system design. It provides an illuminating insight into the sources of EOS in manufacturing, integration of on-chip, and system level EOS protection networks, followed by examples in specific technologies, circuits, and chips.

The book is unique in covering the EOS manufacturing issues from on-chip design and electronic design automation to factory-level EOS program management in today's modern world. Look inside for extensive coverage on: Fundamentals of electrical overstress, from EOS physics, EOS time scales, safe operating area (SOA), to physical models for EOS phenomena EOS sources in today's semiconductor manufacturing environment, and EOS program management, handling and EOS auditing processing to avoid EOS failures EOS failures in both semiconductor devices, circuits and system Discussion of how to distinguish between EOS events, and electrostatic discharge (ESD) events (e.g. such as human body model (HBM), charged device model (CDM), cable discharge events (CDM), charged board events (CBE), to system level IEC 61000-4-2 test events) EOS protection on-chip design practices and how they differ from ESD protection networks and solutions Discussion of EOS system level concerns in printed circuit boards (PCB), and manufacturing equipment Examples of EOS issues in state-of-the-art digital, analog and power technologies including CMOS, LDMOS, and BCD EOS design rule checking (DRC), LVS, and ERC electronic design automation (EDA) and how it is distinct from ESD EDA systems EOS testing and qualification techniques, and Practical off-chip ESD protection and system level solutions to provide more robust systems Electrical Overstress (EOS): Devices, Circuits and Systems is a continuation of the author's series of books on ESD protection. It is an essential reference and a useful insight into the issues that confront modern technology as we enter the nano-electronic era.

It is the main objective of this work to address the scaling and design challenges of ESD protection in deeply scaled technologies. First, the thesis introduces the on-chip ESD events, the scaling and design challenges, and the nomenclatures necessary for later chapters. The ESD design window and the I/O schematics for both rail clamping and local clamping ESD schemes are illustrated. Then, the thesis delves into the investigation of the input and output driver devices and examines their robustness under ESD. The input driver's oxide breakdown levels are evaluated in deeply scaled technologies. The output driver's trigger and breakdown voltages are improved appreciably by applying circuit and device design techniques. The ESD device sections first discuss rail-based clamping, a widely used protection scheme. Two diode-based devices, namely the gated diode and substrate diode, are investigated in detail with SOI test structures. Characterization is based on DC current-voltage (I-V), Very Fast Transmission Line Pulse (VF-TLP), capacitance, and leakage measurements. Improvements in performance are realized. Technology computer aided design (TCAD) simulations help understand the physical effects and design tradeoffs. Then, the following section focuses on the local clamping scheme. Two devices, the field-effect diode (FED) and the double-well FED (DWFED), are developed and optimized in an SOI technology. Trigger circuits are designed to improve the turn-on speed. The advantages of local clamping is highlighted and compared with the rail-based clamping. The results show that the FED is a suitable option for power clamping applications and the DWFED is most suitable for pad-based local clamping. The thesis presents an ESD protection design methodology, which takes advantage of the results and techniques from pervious chapters and put each element into a useful format. Based on the correlation of package level and in-lab test results, a de-

sign process based on CDM target definition and device optimization, discharge path analysis, parasitic minimization, I/O data rate estimation and finally ESD and performance characterization is used sequentially to systematically realize the overall design goals.

Based on the authors' expansive collection of notes taken over the years, Nano-CMOS Circuit and Physical Design bridges the gap between physical and circuit design and fabrication processing, manufacturability, and yield. This innovative book covers: process technology, including sub-wavelength optical lithography; impact of process scaling on circuit and physical implementation and low power with leaky transistors; and DFM, yield, and the impact of physical implementation.

Electrostatic discharge (ESD) continues to impact semiconductormanufacturing, semiconductor components and systems, astechnologies scale from micro- to nano electronics. This bookintroduces the fundamentals of ESD, electrical overstress (EOS),electromagnetic interference (EMI), electromagnetic compatibility(EMC), and latchup, as well as provides a coherent overview of thesemiconductor manufacturing environment and the final systemassembly. It provides an illuminating look into the integration ofESD protection networks followed by examples in specifictechnologies, circuits, and chips. The text is unique in covering semiconductor chip manufacturingissues, ESD semiconductor chip design, and system problemsconfronted today as well as the future of ESD phenomena andnano-technology. Look inside for extensive coverage on: The fundamentals of electrostatics, triboelectric charging, andhow they relate to present day manufacturing environments ofmicro-electronics to nano-technology Semiconductor manufacturing handling and auditing processing toavoid ESD failures ESD, EOS, EMI, EMC, and latchup semiconductor component andsystem level testing to demonstrate product resilience from humanbody model (HBM), transmission line pulse (TLP), charged devicemodel (CDM), human metal model (HMM), cable discharge events (CDE),to system level IEC 61000-4-2 tests ESD on-chip design and process manufacturing practices andsolutions to improve ESD semiconductor chip solutions, alsopractical off-chip ESD protection and system level solutions toprovide more robust systems System level concerns in servers, laptops, disk drives, cellphones, digital cameras, hand held devices, automobiles, and spaceapplications Examples of ESD design for state-of-the-art technologies,including CMOS, BiCMOS, SOI, bipolar technology, high voltage CMOS(HVCMOS), RF CMOS, smart power, magnetic recording technology,micro-machines (MEMs) to nanostructures ESD Basics: From Semiconductor Manufacturing to ProductUse complements the author’s series of books on ESDprotection. For those new to the field, it is an essentialreference and a useful insight into the issues that confront moderntechnology as we enter the Nano-electronic Era.

This volume presents an integrated treatment of ESD, I/O, and process parameter interactions that both I/O designers and process designers can use. It examines key factors in I/O and ESD design and testing, and helps the reader consider ESD and reliability issues up front when making I/O choices. Emphasizing clarity and simplicity, this book focuses on design principles that can be applied widely as this dynamic field continues to evolve.

A thorough and concise treatment of ESD Recognizing its method-

ic, step-by-step attack of theelectrostatic discharge (ESD) problem, the initial release of thisbook was quoted by specialists as "the most thorough and concisetreatment of the broad ESD continuum that is available." Now in itsThird Edition, this book delivers the same trusted coverageof the topic while also incorporating recent technological advancesthat have taken place in the engineering community. The book beginswith the basics of ESD for humans and objects, and goes on tocover: Effects of ESD coupled to electronics Principal ESD specifications ESD diagnostics and testing Design for ESD immunity To help with troubleshooting, many ESD case histories are givenalong with their successful fixes. Electrostatic Dischargeis essential reading for all designers who want to avoid componentfailures, no trouble found incidents, and random errors.

The scaling of semiconductor devices from sub-micron to nanometer dimensions is driving the need for understanding the design of electrostatic discharge (ESD) circuits, and the response of these integrated circuits (IC) to ESD phenomena. ESD Circuits and Devices provides a clear insight into the layout and design of circuitry for protection against electrical overstress (EOS) and ESD. With an emphasis on examples, this text: explains ESD buffering, ballasting, current distribution, design segmentation, feedback, coupling, and de-coupling ESD design methods; outlines the fundamental analytical models and experimental results for the ESD design of MOSFETs and diode semiconductor device elements, with a focus on CMOS, silicon on insulator (SOI), and Silicon Germanium (SiGe) technology; focuses on the ESD design, optimization, integration and synthesis of these elements and concepts into ESD networks, as well as applying within the off-chip driver networks, and on-chip receivers; and highlights state-of-the-art ESD input circuits, as well as ESD power clamps networks. Continuing the author’s series of books on ESD, this book will be an invaluable reference for the professional semiconductor chip and system ESD engineer. Semiconductor device and process development, quality, reliability and failure analysis engineers will also find it an essential tool. In addition, both senior undergraduate and graduate students in microelectronics and IC design will find its numerous examples useful.

Electrostatic Discharge is a pervasive issue in the semiconductor industry affecting both manufacturers and users of semiconductors. This easy-to-read, practical handbook presents an overview of ESD as it effects electronic circuits and provides a concise introduction for students, engineers, circuit designers and failure analysts.

With the evolution of semiconductor technology and global diversification of the semiconductor business, testing of semiconductor devices to systems for electrostatic discharge (ESD) and electrical overstress (EOS) has increased in importance. ESD Testing: From Components to Systems updates the reader in the new tests, test models, and techniques in the characterization of semiconductor components for ESD, EOS, and latchup. Key features: Provides understanding and knowledge of ESD models and specifications including human body model (HBM), machine model (MM), charged device model (CDM), charged board model (CBM), cable discharge events (CDE), human metal model (HMM), IEC 61000-4-2 and IEC 61000-4-5. Discusses new testing methodologies such as transmission line pulse (TLP), to very fast transmis-

sion line pulse (VF-TLP), and future methods of long pulse TLP, to ultra-fast TLP (UF-TLP). Describes both conventional testing and new testing techniques for both chip and system level evaluation. Addresses EOS testing, electromagnetic compatibility (EMC) scanning, to current reconstruction methods. Discusses latchup characterization and testing methodologies for evaluation of semiconductor technology to product testing. ESD Testing: From Components to Systems is part of the authors' series of books on electrostatic discharge (ESD) protection; this book will be an invaluable reference for the professional semiconductor chip and system-level ESD and EOS test engineer. Semiconductor device and process development, circuit designers, quality, reliability and failure analysis engineers will also find it an essential reference. In addition, its academic treatment will appeal to both senior and graduate students with interests in semiconductor process, device physics, semiconductor testing and experimental work.

ESD: Circuits and Devices 2nd Edition provides a clear picture of layout and design of digital, analog, radio frequency (RF) and power applications for protection from electrostatic discharge (ESD), electrical overstress (EOS), and latchup phenomena from a generalist perspective and design synthesis practices providing optimum solutions in advanced technologies. New features in the 2nd edition: Expanded treatment of ESD and analog design of passive devices of resistors, capacitors, inductors, and active devices of diodes, bipolar junction transistors, MOSFETs, and FINFETs. Increased focus on ESD power clamps for power rails for CMOS, Bipolar, and BiCMOS. Co-synthesizing of semiconductor chip architecture and floor planning with ESD design practices for analog, and mixed signal applications Illustrates the influence of analog design practices on ESD design circuitry, from integration, synthesis and layout, to symmetry, matching, inter-digitation, and common centroid techniques. Increased emphasis on system-level testing conforming to IEC 61000-4-2 and IEC 61000-4-5. Improved coverage of low-capacitance ESD, scaling of devices and oxide scaling challenges. ESD: Circuits and Devices 2nd Edition is an essential reference to ESD, circuit & semiconductor engineers and quality, reliability &analysis engineers. It is also useful for graduate and undergraduate students in electrical engineering, semiconductor sciences, microelectronics and IC design.

Provides the understanding and practical skills needed to develop and maintain an effective ESD control program for manufacturing, storage, and handling of ESD sensitive components This essential guide to ESD control programs explains the principles and practice of ESD control in an easily accessible way whilst also providing more depth and a wealth of references for those who want to gain a deeper knowledge of the subject. It describes static electricity and ESD principles such as triboelectrification, electrostatic fields, and induced voltages, with the minimum of theory or mathematics. It is designed for the reader to "dip into" as required, rather than need to read cover to cover. The ESD Control Program Handbook begins with definitions and commonly used terminology, followed by the principles of static electricity and ESD control. Chapter 3 discusses ESD susceptible electronic devices, and how ESD susceptibility of a component is measured. This is followed by the "Seven habits of a highly effective ESD program", explaining the essential activities of an effective ESD control program. While most texts mainly address manual handling of ESD susceptible devices, Chapter 5 extends the discussion to

ESD control in automated systems, processes and handling, which form a major part of modern electronic manufacture. Chapter 6 deals with requirements for compliance given by the IEC 61340-5-1 and ANSI/ESD S20.20 ESD control standards. Chapter 7 gives an overview of the selection, use, care and maintenance of equipment and furniture commonly used to control ESD risks. The chapter explains how these often work together as part of a system and must be specified with that in mind. ESD protective packaging is available in an extraordinary range of forms from bags, boxes and bubble wrap to tape and reel packaging for automated processes. The principles and practice of this widely misunderstood area of ESD control are introduced in Chapter 8. The thorny question of how to evaluate an ESD control program is addressed in Chapter 9 with a goal of compliance with a standard as well as effective control of ESD risks and possible customer perceptions. Whilst evaluating an existing ESD control program provides challenges, developing an ESD control program from scratch provides others. Chapter 10 gives an approach to this. Standard test methods used in compliance with ESD control standards are explained and simple test procedures given in Chapter 11. ESD Training has long been recognised as essential in maintaining effective ESD control. Chapter 12 discusses ways of covering essential topics and how to demonstrate static electricity in action. The book ends with a look at where ESD control may go in the near future. The ESD Control Program Handbook: Gives readers a sound understanding of the subject to analyze the ESD control requirements of manufacturing processes, and develop an effective ESD control program Provides practical knowledge, as well as sufficient theory and background to understand the principles of ESD control Teaches how to track and identify how ESD risks arise, and how to identify fitting means for minimizing or eliminating them Emphasizes working with modern ESD control program standards IEC 61340-5-1 and ESD S20:20 The ESD Control Program Handbook is an invaluable reference for anyone tasked with setting up, evaluating, or maintaining an effective ESD control program, training personnel, or making ESD control related measurements. It would form an excellent basis for a University course on the subject as well as a guide and resource for industry professionals.

With the continuing advancement of semi-conductors, the protection against electrostatic discharge (ESD), the event in which a finite amount of charge is transferred resulting more than 35% of all chip damage and information loss, could not be of higher priority. This book examines ESD concepts, models, protection solutions, and design strategies for on-chip ESD structures. Written by experts in the field, it offers necessary information on the backgrounds, methods, and approaches to the design and development of ESD protection solutions crucial to modern and future electronics.